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Nuclear Instruments and Methods in Physics Research A 409 (1998) 315–321

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Ultra Low Noise CMOS preamplifier-shaper for X-ray spectroscopy

P. O'Connor[a], G. Gramegna[b,*], P. Rehak[a], F. Corsi[b], C. Marzocca[b]

[a] *Brookhaven National Laboratory, Upton, NY 11973, USA*

[b] *Politecnico di Bari, Dipartimento di Elettrotecnica ed Elettronica, via E. Orabona 4, 70100 Bari, Italy*

Abstract

We report here an Ultra Low Noise CMOS charge-sensitive amplifier (CSA) and a CSA-Shaper for X-ray spectroscopy, suitable for a small anode capacitance, low leakage current solid state detector. The continuously sensitive CSA and CSA-Shaper use a MOS transistor MF to discharge the integration capacitance; a novel self-bias circuit biases MF in the GΩ region (subthreshold region) while tracking process, temperature and supply voltage variations. A T-Network in the DC-feedback improves the CSA gain linearity (within 0.1% up to 1.8 fC input charge).

The CSA-Shaper features a novel Adaptive Pole-Zero cancellation scheme: the Zero in the Shaper adapts itself statically and dynamically to cancel the CSA Pole.

The noise performance of the CSA has been measured: with no detector connected and MF pinched, the room-temperature equivalent noise charge (ENC) is 9e rms at 12 μs shaping time. When connected to a cooled detector ($T = -75$°C), with MF in pinch off, an ENC of 13e rms is achieved (FHWM = 111 eV) at 2.4 μs shaping time. This is the best reported energy resolution ever obtained with a CMOS preamplifier.

Keywords: CMOS preamplifier-shaper; X-ray spectroscopy; Adaptive pole-zero suppression; Adaptive bias circuit; Best reported noise performance in CMOS

1. Introduction

For ultra low noise applications, front-end circuits matched to detectors with small anode capacitance and low leakage current are used. The charge-sensitive amplifier (CSA) is widely used, as its voltage–charge gain is independent of anode capacitance variations (Fig. 1). The signal charge is integrated on a capacitance CF, which has to be discharged to prevent the preamplifier from being saturated by subsequent integration events and the detector leakage current. The technique used to discharge CF influences significantly on the performance of ultra low noise systems [1,2].

Three approaches have been proposed so far for the front-end circuit. The first one is the integration of the input transistor of the preamplifier into the detector itself to avoid the capacitance associated with the connections [3]. This approach gave the best performance so far [4], but its drawback is the fabrication of the CSA's input transistor with all the constraints imposed by the production of high-quality detectors. As a consequence: (i) the first transistor is not optimized, (ii) the introduction of additional masks reduces the yield of the process

* Corresponding author. Tel.: + 39 80 5460 313; fax: + 39 80 5460 410; e-mail: giuse@deeetr02.poliba.it.

0168-9002/98/$19.00
PII S0168-9002(97)01289-8

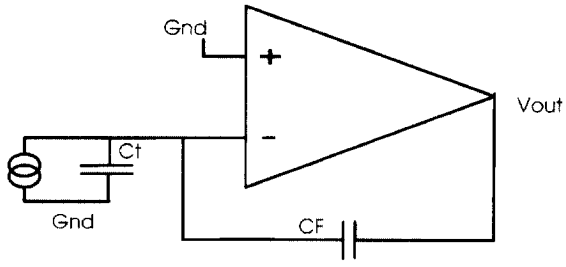


Fig. 1. Charge-Sensitive Amplifier (CSA) based on a core voltage amplifier with shunt feedback.

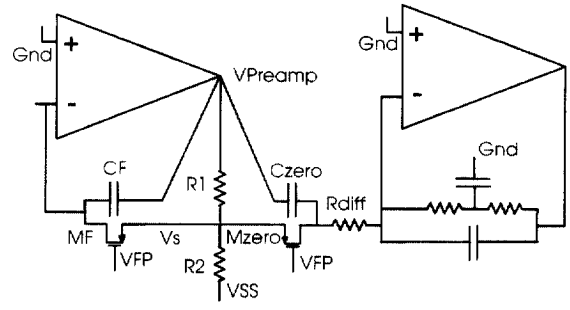


Fig. 2. CSA (left-hand side) and Shaper circuit.

(iii), the integrated transistor increases the usually negligible anode capacitance.

The second approach is to use an external JFET as input transistor of the CSA. An X-ray system presently under test implements a novel feedback scheme by using a JFET transistor with input capacitance of 0.5 pF [5].

The third approach is the use of a monolithic CMOS preamplifier [6–8]. A *P*-channel input device is mandatory to benefit from the lower flicker noise (compared to a *N*-channel one). The use of low-cost CMOS technology calls for adhoc design techniques. In this paper we report novel circuit techniques and their implementation on a CMOS front-end circuit for ultra low noise applications.

2. Circuit techniques

To establish the DC path, a resistance R can be inserted in parallel to the integration capacitance CF. R does not contribute to the parallel noise if $4\,kT/R \ll 2\,qI_{leak}$. Ultra low noise systems require detectors with leakage currents $1\,pA < I_{leak} < 100\,pA$, thus R must be in the range. $5\,G\Omega < R < 50\,G\Omega$. The only possible way to realize such a high resistance in CMOS technology is by using a MOS transistor. To fully benefit from the small anode capacitance, a minimum size feedback device with negligible parasitics added to the input node is required. These requirements set the biasing condition of MF in the subthreshold region, where its associated resistance R_{ds}(MF) changes exponentially with the bias potentials.

The use of such device in the feedback loop necessitates the solution of three issues: (i) how to bias MF in the GΩ range, and stabilize its DC resistance against process, temperature and supply voltage variations (in particular, the threshold voltages can change ± 100 mV from chip to chip); (ii) how to improve the linearity of a system with a non-linear resistance in the feedback loop. The worsening is due to the change of the decay time during the transient and its dependence upon the integrated charge. Finally (iii) how to stabilize the voltage–charge gain versus the detector leakage current.

We addressed those issues by using novel circuit techniques. The techniques have been implemented in a CSA [9] and a CSA-Shaper fabricated in two different technologies (HP 1.2 μm and AMS 1.2 μm).

2.1. T-network in the DC feedback

In a real CSA, the signal charge is integrated onto CF with a rise time T_{rise} and discharged with a decay time T_{decay} imposed by the feedback network. The voltage–charge gain, which in the ideal case is 1/CF, is reduced when the ratio T_{decay}/T_{rise} is not sufficiently high. In such conditions, a variation of T_{decay} results in a variation of the voltage–charge gain.

In our case R_{ds}(MF) depends exponentially upon the biasing conditions of MF, thus its value changes during the discharge of CF. If CF = 15 fF, with $Q_{in} = 0.75$ fC the output swings of 50 mV which, if applied to the V_{gs}(MF) would change

R_{ds}(MF) of a factor four. To improve the linearity of the voltage–charge gain we inserted a voltage divider between the output of the preamplifier and the source of MF (Fig. 2). Consequently, the R_{ds}(MF) variation during the dynamic swing is attenuated. Moreover, $T_{decay} = k*R_{ds}(MF)*CF$, i.e. the ratio T_{decay}/T_{rise} is increased by a factor $k = (R1 + R2)/R2$.

We measured the voltage–charge gain using a on-chip injection capacitance and a Multichannel Analyzer. The CSA gain (G = 80 mV/fC) is linear within 0.1% up to 1.8 fC input charge.

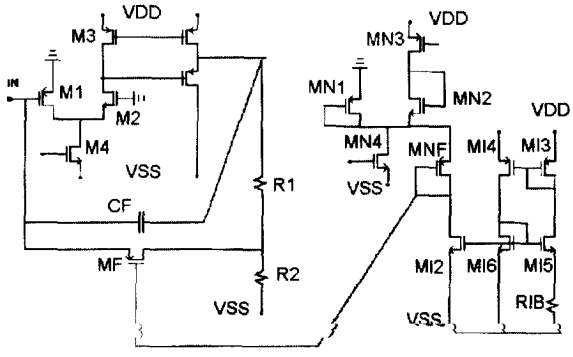


Fig. 3. CSA (left-hand side) and Self-Bias circuit for MF.

2.2. Self-adaptive bias circuit for MF

We developed and implemented the Self-Adaptive bias scheme for a CMOS CSA with N-channel input device, matched to 0.8 pF detector capacitance, to be used for a particle tracking system [10,11]. In that application the peaking time was 50 ns, and we achieved a feedback resistance of 6 MΩ with a $W/L = \frac{3}{20}$ MOS device biased in the triode strong inversion region.

In the present application the problem is similar, but the scheme must be modified for use with a P-channel input device. Moreover, the requirements are more challenging: we are forced to use a minimum size MOSFET device (W/L = 3 μm/3 μm) biased in the subthreshold region, with an associated resistance three orders of magnitude larger (GΩ region). This makes R_{ds}(MF) extremely sensitive to the biasing condition of MF and on the threshold voltages. The issue has been addressed by modifying the self-adaptive scheme for a P-channel input device and improving its capability to track threshold variations. The circuit shown in Fig. 3 keeps V_{gs}(MF)–V_{th}(MF) = const., even when V_{gs}(MF) is only a few times kT/q below threshold.

The gate voltage V_g(MF) tracks the variations in V_{th}(M1) and V_{th}(MF): a diode-connected replica MN1 of M1 is biased at the same current density so that the voltage at the drain of MN1 tracks the NMOS threshold (V_g(MN1) = V_g(M1)). Moreover, the required gate-to-source voltage of the feedback device is generated by passing a current I_d(MNF) through the diode MNF. MNF is a scaled copy of MF created by laying out n parallel copies of MF. Since MNF has the same V_{bs} and width as MF, it experiences the same body and narrow-channel effects which affect V_{th}(MF). It results that V_{th}(MF) = V_{th}(MNF) and

$$V_{gs}(MF) - V_{th}(MF) = V_{gs}(MNF) - V_{th}(MNF) = F(I_{ds}(MNF)).$$

In other words, the biasing conditions of MF are set by the current I_{ds}(MNF) (which can be controlled within 20%) rather than by the threshold voltages, which influence R_{ds}(MF) exponentially.

In this circuit the number of MF's copies we use to lay-out MNF is n = 180. The low-current source (MI2–MI6, RIB in Fig. 3) set I_d(MNF) = 12 nA.

In Fig. 4 the CSA response to charge pulse at different temperature is shown. In the 100°C temperature range V_{th}(MF) change of 100 mV and R_{ds}(MF) would change of two orders of magnitudes. The self-adaptive bias circuit tracks the threshold voltage and dR_{ds}(MF)/R_{ds}(MF) = 20%.

The CSA output is moved positive by the detector leakage current I_{leak} and the node V_s (right-hand side of MF) becomes MF's effective source. The consequent reduction of R_{ds}(MF) (proportional to I_{leak}) extends the range of the allowable I_{leak} current from the detector. Clearly a higher value of I_{leak} degrades the energy resolution.

It's possible to force on the node VFP (gate of MF) bias conditions different from the natural one. This feature was used to obtain the best possible noise performance.

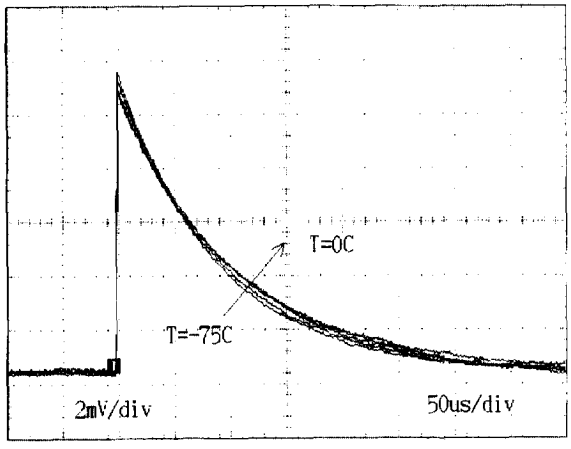


Fig. 4. Response of the CSA to a charge signal at different temperatures (− 75°C, − 50°C, − 25°C, 0°C, 25°C).

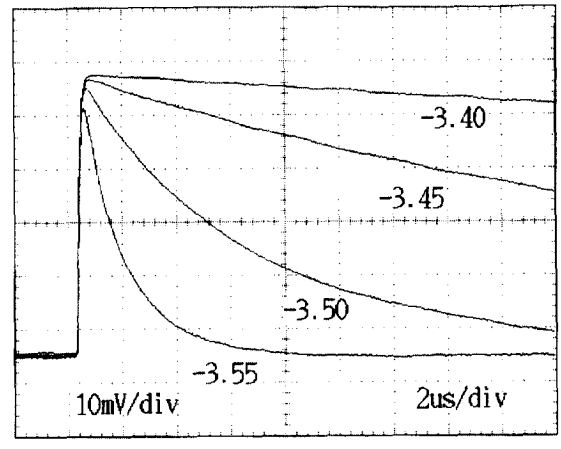
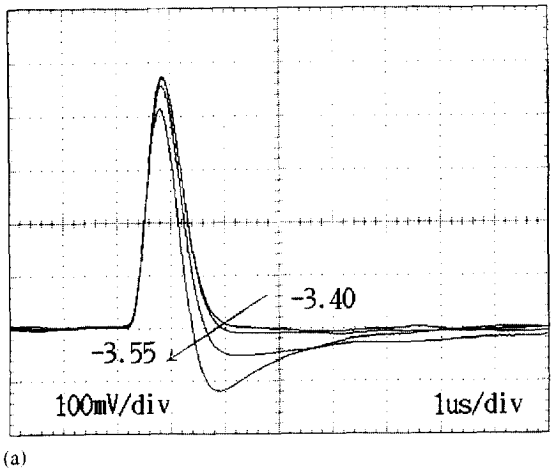


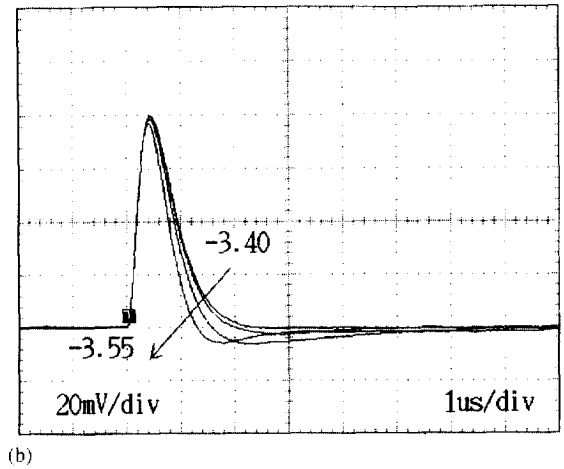
Fig. 5. CSA response to a charge signal for different V_{FP} forced to the gate of MF (− 3.40, − 3.45, − 3.50, − 3.55) V, i.e. feedback resistances.

2.3. *Adaptive Pole-Zero cancellation in the CSA-shaper*

The new scheme, a variation of the one implemented in Refs. [9,10], is based on the classical Pole-Zero cancellation technique [12]. With reference to Fig. 2, M_{zero} is biased in the same way as MF for every value of I_{leak} and every value of V_{Preamp}. Consequently, the *variations* of $R_{ds}(M_{zero})$ and R_{ds}(MF) during the discharge of CF are the same. In other words, the Zero associated with the network C_{zero}–M_{zero} adapts itself *statically* and *dynamically* to accurately cancel the preamplifier pole. The response of the preamplifier to a charge event with various VFP forced to the gate of MF (i.e. various feedback resistances) is reported in Fig. 5. The corresponding responses of the CSA-External Shaper and CSA-Shaper (Fig. 6) prove the effectiveness of the scheme: the adaptive Pole-Zero cancellation makes the response of the CSA-Shaper independent on the position of the CSA Pole.



(a)



(b)

Fig. 6. (a) CSA-external Shaper and (b) CSA-Shaper response to a charge signal at various V_{FP} forced to the gate of MF and M_{zero}.

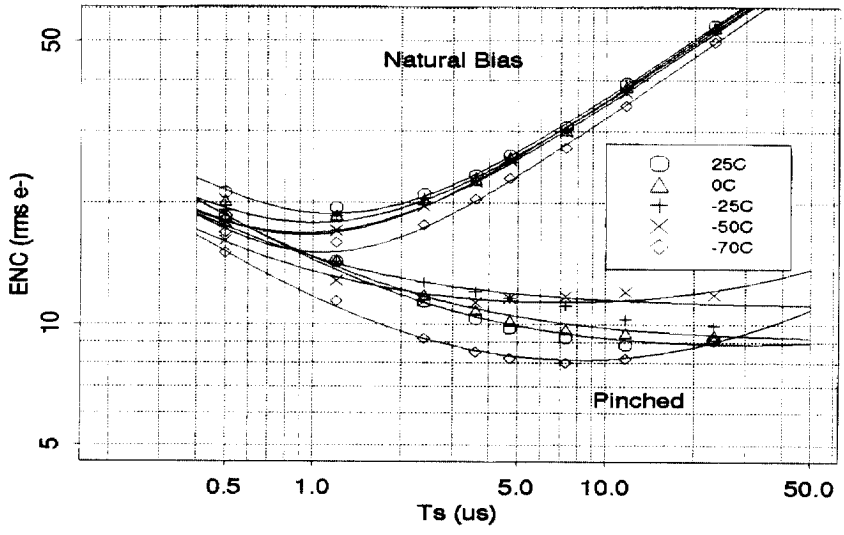


Fig. 7. ENC versus shaping time for the AMS CSA at various temperatures (CSA not connected to detector). MF self-biased (upper group) and MF pinched-off (lower diagrams).

3. Noise performance of the CSA

We measured the ENC versus shaping time for various temperatures in two bias conditions of MF: pinch-off, and the one imposed by the self-adaptive bias circuit (1.8 GΩ). As far as the pinched state is concerned, an increase of the gate voltage of the feedback device MF by about 15 mV from the self-biased condition, brings MF's effective resistance to about 100 GΩ. Under these conditions, the parallel noise is almost eliminated, as seen in Fig. 7. However, the circuit is still stable and continuously sensitive and can be maintained in this condition without adjustment of the gate voltage for up to 12 h; this is sufficient for most spectroscopy runs. The only practical use of the CSA in this pinched condition is with detectors having $I_{leak} < 1$ pA. With no detector connected, we measure an ENC of 9e rms at room temperature.

The CSA, connected to an external Shaper, has been coupled to a Silicon Drift Detector (SDD) [13] cooled down to $T = -75°C$. The capacitance of the SDD anode plus the parasitics associated with the bond wire are estimated equal to 600 fF. With $t_s = 2.4$ μs shaping time and MF in pinch-off, the spectrum of ^{241}Am and ^{55}Fe has been taken (Figs. 8 and 9). We measure FHWM = 111 eV (ENC = 13e rms), which is an improvement of almost a factor of 2 over the best previously reported resolution of a Si detector coupled to a CMOS circuit [6,7]. The noise performance is summarized in Table 1.

These noise performances have been achieved with a preseudo-Gaussian Shaper with the CSA's noise dominated by the flicker noise of M1 (long shaping time, low I_{leak}). An optimal filter for flicker noise improved the energy resolution by 18% [14,15]: we estimate that with such a filter our CSA connected to a detector can reach 11e rms.

The noise performance of the CSA-Shaper was not measured.

4. Conclusions

Novel circuit techniques have been implemented in an ultra low noise CSA and a CSA-Shaper fabricated in two different technologies (HP 1.2 μm and AMS 1.2 μm).

The CSA and CSA-Shaper are continuously sensitive and require no external components or adjustment to be operated. In its self-biased

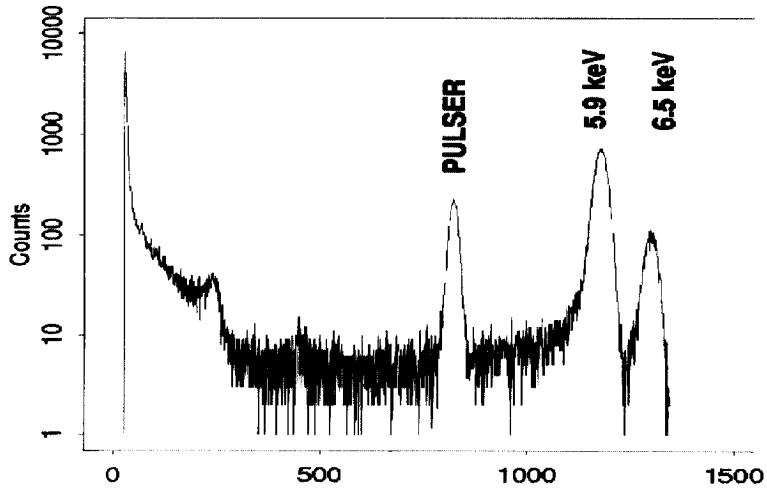


Fig. 8. ^{55}Fe Spectrum of the AMS CSA at − 70°C (log vertical scale). FHWM = 111 eV (13e rms).

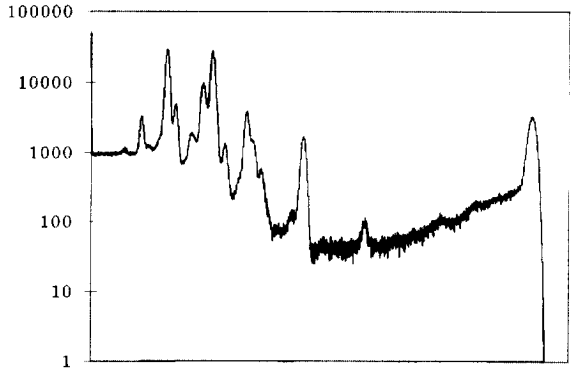


Fig. 9. ^{241}Am Spectrum of the AMS CSA at − 70°C (log vertical scale).

Table 1
Noise performance of the CSA for various operating conditions

ENC (e rms)	T_s (μs)	Detector	Cooled	Pinched
19	1.2	No	No	No
14	1.2	No	Yes	No
9	12	No	No	Yes
8	8	No	Yes	Yes
13	2.4	Yes	Yes	Yes

condition, the AMS version has 1.8 GΩ feedback resistance. The linearity of the CSA voltage–charge gain has been improved by using a T-Network for the DC feedback (within 0.1% up to 1.8 fC input charge).

The CSA-Shaper uses an Adaptive Pole-Zero cancellation technique to accurately cancel the CSA Pole.

The best noise performance is obtained with MF pinched off, no detector connected, and with the circuit cooled to − 70°C. Under these conditions the ENC is 8e rms at a shaping time of 8 μs, limited entirely by the flicker noise of the input transistor. This increases to 14e rms if we allow MF to be biased by the self-adaptive circuit. With a cooled SDD connected, a FWHM of 111 eV is obtained at 2.4 μs corresponding to an ENC of 13e. The noise performance is the best ever achieved with a CMOS preamplifier.

Acknowledgements

The authors wish to thank D. Pinelli and F. De Candia for their excellent technical support, and V. Radeka for his guidance and encouragement of this project. G. Gramegna wished to thank V. Radeka for his hospitality at BNL.

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